Industry and Sustainable Nanotechnology

How can nanotechnology make industry more sustainable?

A semiconductor industry perspective

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Semiconductor Research Corporation

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General ways nano impacts industry sustainability

• Green(er) synthesis of (nano)materials and (nano)structures
  – Bottom up or additive fabrication
  – Improved sensing and filtration
• Synthesis of green(er) (nano)materials and (nano)technologies
  – Less is more, e.g. surface-driven applications
• Improved functionality, often in a smaller package
Nanotechnology for Medicine

- Imaging
- Diagnostics
- Therapeutics


Source: NIST
Credit: J. Chang, Vanderbilt
Most drugs...don’t work for most people...most of the time.
Nanotechnology for Living

• Assistive Technologies
• Health monitors


Nanotechnology for Automotive

“Edison2 combines sound physics with innovative design to produce workable and sustainable transportation solutions.”

http://www.edison2.com/
Nanotechnology for Energy

- Solid state lighting
- Solar cells
- Batteries
Nanotechnology for ITC & Electronics

• More connected
• More mobile
• More data = more knowledge
• More “intelligent” environment
Semiconductors Enable Broad Energy Efficiency
Save 1.2 Trillion kWh, Reduce CO₂ emissions by 733 MMT in 2030

No Further Efficiency Improvements

DOE Baseline Projection

1.9 Trillion kWh Savings Planned

1.2 Trillion kWh Below Plan

*Note: Accelerated investments in semiconductor-related technologies stimulated by smart policies.
Nanotechnology for Semiconductors

- Nanomaterials
- Nanostructures
- Nanomanufacturing
- Nano metrology & characterization
Moore’s Law: # transistors/chip doubles every 24 months
1982: Best available storage technology was the IBM 3350

126 IBM 3350’s = storage in 1 iPod

Each unit:
- 635 MB
- $70,000

80Gb cost $9,000,000 !!! in 1976 dollars

In 2012:
- 80Gb cost $100 in 2012 dollars
- iPod(5G) 80GB
Nanotechnology + Electronics = Today’s Semiconductor Industry
Nano-thick Gate Oxide Layer Requires New High-K Material

<table>
<thead>
<tr>
<th>Material</th>
<th>$K$</th>
<th>Gap (eV)</th>
<th>CB offset (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td></td>
<td>1.1</td>
<td></td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>3.9</td>
<td>9</td>
<td>3.2</td>
</tr>
<tr>
<td>Si$_3$N$_4$</td>
<td>7</td>
<td>5.3</td>
<td>2.4</td>
</tr>
<tr>
<td>Al$_2$O$_3$</td>
<td>9</td>
<td>8.8</td>
<td>2.8 (not ALD)</td>
</tr>
<tr>
<td>Ta$_2$O$_5$</td>
<td>22</td>
<td>4.4</td>
<td>0.35</td>
</tr>
<tr>
<td>TiO$_2$</td>
<td>80</td>
<td>3.5</td>
<td>0</td>
</tr>
<tr>
<td>SrTiO$_3$</td>
<td>2000</td>
<td>3.2</td>
<td>0</td>
</tr>
<tr>
<td>ZrO$_2$</td>
<td>25</td>
<td>5.8</td>
<td>1.5</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>25</td>
<td>5.8</td>
<td>1.4</td>
</tr>
<tr>
<td>HfSiO$_4$</td>
<td>11</td>
<td>6.5</td>
<td>1.8</td>
</tr>
<tr>
<td>La$_2$O$_3$</td>
<td>30</td>
<td>6</td>
<td>2.3</td>
</tr>
<tr>
<td>Y$_2$O$_3$</td>
<td>15</td>
<td>6</td>
<td>2.3</td>
</tr>
<tr>
<td>a-LaAlO$_3$</td>
<td>30</td>
<td>5.6</td>
<td>1.8</td>
</tr>
</tbody>
</table>

As Transistors Shrink, So Do Interconnects

Half of microprocessor power goes to interconnects (> 1 billion transistors; total budget = 200 watts)

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate</td>
<td>34%</td>
</tr>
<tr>
<td>Interconnect</td>
<td>51%</td>
</tr>
<tr>
<td>Diffusion</td>
<td>15%</td>
</tr>
</tbody>
</table>

New conductive and insulating (nano)materials are needed

Length of interconnects in a microprocessor = 36 miles

Source: NIST
Interconnect Triple Challenge

Cu line resistivity (micro-ohm-cm)

barrier thickness (nm)

ILD Bulk dielectric constant

Source: J. Clarke, Intel

Need Better (Nano)Insulators: Low-k Dielectric Materials

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>Value of $k$ (@ 1 MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_x$ F$_y$</td>
<td>3.2 - 3.5</td>
</tr>
<tr>
<td>Hydrogen silsesquioxane</td>
<td>3.0</td>
</tr>
<tr>
<td>Polysiloxane</td>
<td>2.89</td>
</tr>
<tr>
<td>Fluoropolyimide</td>
<td>2.8</td>
</tr>
<tr>
<td>Benzo-cyclo-butane</td>
<td>2.7</td>
</tr>
<tr>
<td>Black diamond</td>
<td>2.7</td>
</tr>
<tr>
<td>Polyethylene</td>
<td>2.4</td>
</tr>
<tr>
<td>Polypropylene</td>
<td>2.3</td>
</tr>
<tr>
<td>Fluoropolymer</td>
<td>2.24</td>
</tr>
<tr>
<td>Perylene</td>
<td>2.2</td>
</tr>
<tr>
<td>Dupont PTFE-based copolymer AF 2400</td>
<td>2.06</td>
</tr>
<tr>
<td>Xerogels</td>
<td>1.2</td>
</tr>
<tr>
<td>Air</td>
<td>1.0</td>
</tr>
<tr>
<td>Carbon dioxide</td>
<td>1.0</td>
</tr>
</tbody>
</table>
“Silicon” Chips are Complex Nanomaterials

What are the possible ESH effects?

Source: Intel
2011 ITRS*: Addressing Increasing Complexity, ESH & Sustainability

• ESH strategies
  – To understand (characterize) processes and materials during the development phase
  – To use materials that are less hazardous or whose byproducts are less hazardous
  – To design products and systems (equipment and facilities) that consume less raw materials and resources
  – To make the factory safe for employees

* International Technology Roadmap for Semiconductors available at www.itrs.org
2011 ITRS: ESH Difficult Challenges (examples)

• Chemicals & materials
  – Assessment/characterization tools & methods
  – Comprehensive ESH data

• Process & equipment
  – “Greener” processes (more benign & less materials)
  – Exposure management

• Facilities
  – Improve efficiency (electricity, water, HVAC)

• Sustainability
  – Design for ESH (similar to other DFX)
  – Need for metrics
2011 ITRS: ESH & Emerging Nanomaterials

• Developing effective monitoring tools to detect nanomaterials’ presence in the workplace, in waste streams, and in the environment

• Evaluating and developing appropriate protocols to ensure worker health and safety

• Evaluating and developing emission control equipment to ensure effective treatment of nanomaterials-containing waste streams

• Understanding new nanomaterials’ toxicity as it may differ from the bulk forms; involves developing rapid nanomaterials toxicity assessment methods as well as nanomaterials toxicity models
Industry’s Voluntary Steps toward Sustainability

- World Semiconductor Council initiatives to reduce environmental impact
  - *Reduce GHG emissions* per area of Si wafer by 30% by 2020 from 2010 levels
  - *Eliminate PFOS* (perfluorooctyl sulfonates) from non-critical applications and research alternatives for critical uses

- Industry goal to keep energy/water use and air emissions constant per wafer during transition from 300 mm to 450 mm (more than 2X area)
Individual Companies Setting Goals:

Intel’s 2012 Environmental Goals

• *Reduce water use* per chip below 2007 levels by 2012
• *Reduce absolute global-warming gas footprint* by 20% by 2012 from 2007 levels
• *Reduce energy consumption* per chip 5% per year from 2007 through 2012
• *Reduce generation of chemical waste* per chip by 10% by 2012 from 2007 levels
• *Recycle 80% of chemical and solid waste* generated per year
• Achieve engineering and design milestones to ensure that Intel products *maintain the energy-efficiency lead* in the market for next two product generations
Individual Companies Setting Goals: TI 2012 Environmental Goals

- Reduce GHG emissions per chip produced 30% by 2015 from 2010 level
- Raise waste efficiency (recycling) rate to 95% (currently 92%)
- Reduce chemical use in manufacturing by 3%
Center for Environmentally Benign Semiconductor Manufacturing

NSF ERC; co-funded with industry (SRC and SEMATECH) for 10 years; industry funded since 2006

APPROACH

✓ Focus on fundamental research to address manufacturing needs and technology gaps
✓ Transfer results to commercial application
✓ Create synergy and partnership with industry in funding and conduct of research

Enabling ESH Fundamentals

Environmentally Sustainable Electronics Manufacturing

Thrust A
Novel Solutions to Existing ESH Problems

Thrust B
ESH-Friendly Novel Materials and Processes

Thrust C
ESH Aspects of Future Nanoscale Manufacturing
Founding Universities
• U Arizona
• U California – Berkeley
• MIT
• Stanford

Other University members
• Arizona State U (1998- )
• Columbia (2006-2009)
• Cornell (1998- )
• Georgia Tech (2009- )
• U Maryland (1999-2003)
• U Massachusetts (2006-2009)
• UNC-Chapel Hill (2009- )
• Purdue (2003-2008 )
• U Texas-Dallas (2009- )
• Tufts (2005-2008 )
• U Washington (2008-)
• U Wisconsin (2009- )
• UCLA (2011- )
• Johns Hopkins (2011- )
• NC A&T (2011- )

CEBMS Stats

Cumulative Data:
19 Core member Universities
243 PhD and MS
205 Undergraduates (reported)
13 Academic disciplines

> 80% of graduates joined SC industry & suppliers (mostly ERC members)

13 Current member universities
37 Current PI/Co-PIs
39 Current graduate students

http://www.erc.arizona.edu/
Use initial cold rinse to flush tank
Use hot water to finish flush and heat wafers
Cycle time is not increased
Savings: ~ 25% cold water and ~ 80% hot water
Technology transferred to industry
Environmentally Friendly (PFOS-Free) Materials for Next Generation Photolithography

1st & 2nd Generation

- Polar
- Hydrophilic
- Aromatic
- Linear
- Branch
- Ring

3rd Generation

- Sugar based
  “Sweet” PAG

- Natural molecule-based
  Biocompatible/
  Biodegradable PAG

1st & 2nd Generation

- Nonpolar
- Hydrophobic
- Aliphatic
New Techniques for Toxicity Assessment of Nanomaterials

Impedance-based method

- HfO$_2$, ZrO$_2$ and CeO$_2$ NPs show mild to no toxicity.
- Higher toxicity correlated to chemical contamination
- Chemical reactive oxide species (ROS) production indicative of NP toxicity
- NPs producing ROS in water are most toxic.

Cell-based method (HBE lung cells)

Time: 0 h 0.5 h 1.0 h 1.5 h 2.0 h

HfO$_2$

- 0 ppm
- 250 ppm
Goal: Understand the factors that impact and reduce single-walled carbon nanotube (SWNT) toxicity.

Approach: Develop standard sonication and centrifugation processes to disperse SWNTs and assess their impact on the proliferative ability of a standard cell line.

Results:

- SWCNT toxicity tends to correlate with contaminants, such as oxidized amorphous carbon species.
- Removal of these toxic contaminants appears to reduce the toxicity associated with carboxylated SWNTs.
Nanoelectronics: Beyond Today’s Technology

• Can we store and send 1’s and 0’s using something other than charge?
• Are there materials that offer advantages?

Carbon Nanotubes

Graphene
Carbon nanotube properties make them candidates to replace CMOS in transistor.

Challenges include:

- Making/sorting homogenous semiconducting material
- Precise placement of nanotubes
- Scalable process
Carbon Nanotube Electronics

IBM researchers have discovered how to:
• precisely place carbon nanotubes on a computer chip,
• arrange the nanotubes 100 times more densely than earlier methods, and
• build a chip with more than 10,000 carbon nanotube-based elements

Over 40 Universities in 19 States
NRI: Research on Novel Materials and Devices for “Beyond Moore’s Law”

Spin-Wave Device
WIN - UCLA, UCSB

Spin-Torque Device
WIN - UCI

Spin-FET
WIN - UCLA

Graphene PN Junction Device
INDEX - SUNY Albany

Graphene Integration
INDEX – SUNY Albany

All-Spin Logic
INDEX - Purdue U.

Graphene Processes
SWAN – UT Dallas

Nanomagnet Logic
MIND - Notre Dame
WIN - Berkeley

Tunnel Devices
MIND

Heterojunctions
Notre Dame, Penn State

Win - UCLA

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Looking Ahead

• Sustainable industry and sustainable nanotechnology go hand in hand

• Areas where work is needed:
  – Nano metrology/characterization
  – Nanomanufacturing
  – Nano sensors
  – Sustainability metrics
Take Away Messages

- Industries are keenly interested in sustainability from a business perspective
- Nanotechnology offers the potential to reduce use of resources and make new greener products
- Nanoelectronics (aka semiconductor industry) has potential to raise sustainability of many other industries